REMARKS

Claims 1-22 are presented for examination. Claims 1, 5, and 17 have been amended.

Claim Objections

Claims 1, 5, and 17 are objected to because of certain informalities. Claims 1, 5, and 17 have been amended to remove the informalities.

Claim Rejections under 35 USC § 112, First paragraph

Claims 2-5, 10-16, and 19 are rejected under 35 U.S.C. 112, first paragraph, as falling to comply with the enablement requirement. Applicants respectfully traverse these rejections.

Claims 2, 10, and 19 have been rejected for reciting the limitation of a remote memory unit comprising dedicated queue for each of the second queue. The specification clearly defines the remote memory unit in various places. For example, in the paragraph beginning at line 15 on page 42, the remote memory device is described as off-chip SDRAM or similar device. Further, in the paragraph beginning at line 10 on page 44, the specification describes moving cells in and out of the SDRAM from the cache 615. Furthermore, paragraphs beginning at line 15 on page 44 and at line 8 on page 45 describe the external memory (e.g., SDRAM) and external queues in the external memory unit SDRAM. Applicants have amended the specification in accordance with MPEP §2163.06 (III) to include the claim language in the specification. No new matter has been added.

Applicants believe that the amended specification adequately describes the remote memory unit and dedicated queues to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Accordingly, Applicants

respectfully request the withdrawal of the rejections of claims 2, 10, and 19 under 35 USC §12, first paragraph.

Claims 3-5 and 11-16 have been rejected for incorporating the limitations of the remote memory unit by their dependency. Accordingly, Applicants respectfully request the withdrawal of the rejections of claims 3-5 and 11-16 under 35 USC §12, first paragraph.

Claim Rejections under 35 USC § 102(e)

Claims 1, 7, 9, 17-18, and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Janoska et al., US 6,539,024 B1. Applicants respectfully traverse these rejections.

Janoska et al. does not anticipate claim 1. To anticipate a claim, the reference must teach each and every element of the claim. *See* MPEP §2131.

First, Janoska et al. does not show a first queue and a plurality of second queues where the first queue is configured to receive a PDU from a communication network as recited in claim 1. The Examiner has cited elements 20-27 in figure 1 of Janoska as queues stating that "the first queue **may be considered** 20, and the second queues 21-27" (emphasis added). Applicants respectfully disagree. The elements 20-27 are "queuing elements" configured to independently receive cells/packets from the associated group of line cards 10. The queuing elements 20-27 are not queues configured to store data. According to Janoska et al., "[n]ote that the output buffer 40 includes a plurality of queuing elements 20-27, where each queuing element receives data cells from a different set of line card input." (*See* col. 3, lines 20-25, emphasis added). In Janoska et al., each queuing element is coupled to its own group of incoming line card 10 via lines 1-15 such as, inputs 12 and 14 for the queuing element 20. In contrast, claim 1 recites that the first queue is configured to receive a PDU from said communication network. Thus, Janoska et al. does not disclose, teach, show, or even suggest that one queue receives the incoming PDUs.

Further, the incoming PDUs in Janoska et al. are stored in an array of logical queues within each queuing elements. According to Janoska et al., "... an array of logical queues is utilized to map received data cells to the limited **buffering space within each of the queuing**

elements." (*See* col. 3, lines 5-8, emphasis added). The array of logical queues and the queuing elements are two distinct elements and as explained by Janoska et al., each queuing element has its own array of queues. Furthermore, figure 4 of Janoska et al., and the corresponding text in col. 5, lines 28-50, explain that each queuing element 20-27 includes the buffer 100, which is divided into various partitions. Therefore, contrary to the Examiner's assertion, each queuing element cannot be considered as individual queue corresponding to the first queue and the plurality of second queues as recited in claim 1. Accordingly Janoska et al. does not show a first queue and a plurality of second queues where the first queue is configured to receive a PDU from a communication network as recited in claim 1.

Second, Janoska et al. does not show the cell buffer indicator as recited in claim 1. The Examiner has cited a "depth pointer" corresponding to each logical queue in Janoska et al. The "depth pointer" of Janoska et al. monitors the space in the corresponding queue and does not issue a first status signal and a second status signal as recited in claim 1. According to Janoska et al., "[a] depteh pointer 144 monitors the number of data cells enqueued in a particular logical queue 62, and decremented each time a data cell is dequeued from the logical queue 62." (*See* col. 7, lines 12-17 and figure 6, emphasis added). Each queue 62 has its own depth pointer 144 and the depth pointer 144 is basically a counter configured to count the number of cells queued in the corresponding queue. In contrast, claim 1 recites a cell buffer indicator that is configured to issue a first queue status signal and a second queue status signal wherein said first queue status signal indicates an occupancy status of said first queue and said second queue status signal indicates an occupancy status of said plurality of second queues. Therefore, the "depth pointer" of Janoska et al. counts the number of cells occupied in a corresponding queue and the cell buffer status indicator as recited in claim 1 indicates the occupancy status of a first queue and a second queue. Accordingly, Janoska et al., does not describe, show, teach, or even suggest the cell buffer status indicator as recited in claim 1.

Third, the Examiner have not provided any citation in Janoska et al. disclosing a cell buffer controller as recited in claim 1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051,

1053 (Fed. Cir. 1987). *See also* MPEP §2131. The Examiner has generally focused on the function of forwarding a PDU from the first queue to a high or low priority queue and has not cited a cell buffer controller in Janoska et al. Accordingly, Janoska et al. does not describea cell buffer controller as recited in claim 1.

As to the general function of forwarding a PDU received in said first queue to one of said plurality of second queues, the Examiner has stated that "the queues may be daisy-chained and therefore the priority applies to forwarding from first to second queues." Applicants respectfully disagree. As explained above, Janoska et al. does not have a first queue and a plurality of second queues. Thus, the incoming PDUs cannot be forwarded in the manner recited in claim 1.

Further, in Janoska et al., the incoming PDUs are received by each queuing element independently and are stored directly into the logical queues according to their priorities and are not transferred to another queue. Furthermore, contrary to the Examiner's assertion, Janoska et al. does not describe that the daisy chain structure is used to transfer PDUs from one queue to another queue based on their priorities. According to Janoska et al., the inter-coupling of queuing elements is for generating the output data stream at output 52 for the output line cards 50 (*see* col. 3, lines 40-53). Thus, Janoska et al. does not describe, show, teach, or even suggest a cell buffer controller operably configured to forward a PDU received in the first queue to one of the plurality of second queues and the PDU is forwarded to one of the high priority queue and the low priority queue in accordance with an appended PDU priority indicator as recited in claim 1.

Therefore, Janoska et al. does not describe, show, teach, or suggest each and every element of claim 1. Accordingly, claim 1 is patentably distinguishable from Janoska et al.

Claim 17 has been rejected in the manner of claim 1. Accordingly, claim 17 is patentably distinguishable from Janoska et al. for at least the same reasons as claim 1. Further, as to claim 17, the Examiner has stated that "shared portion is seen as the remote." The shared portion of a partition is not remote from the reserved portion. Applicants would like to point to the Examiner that the shared portion of a partition is not remote from the buffer itself but it is a shared storage area within the partition. According to Janoska et al., each queuing element 20-27 includes a buffer 100 (*see* col. 5, lines 30-33). The buffer 100 is divided into a number of

different partitions (*see* col. 5, lines 35-37 and figure 4). Further, each partition includes reserved portions and share portion (*see* figure 5). The reserved portions **within** a given partition (partition 102 shown in figure 5) are assigned to individual logical queues that map to that particular partition (*see* col. 6, lines 5-11) and shared portion within the same partition is used by all of the logical queues that map to that particular partition (*see* col. 6, lines 29-32). The shared portion of a partition is not remote from the reserved portion. In fact, the shared portion is actually part of the same partition and is used to store the overflow data from each reserved portion within the same partition.

Furthermore, Janoska et al. states that "the reserved portion of a partition is **optional**, and the entire resource base of the partition may be shared amongst all the logical queues corresponding to the partition." (*See* col. 6, lines 43-46). Therefore, contrary to the Examiner's assertion, the shared portion of a partition cannot be seen as remote. Accordingly, claim 17 is further patentably distinguishable from Janoska et al.

Claims 7 and 9 depend from claim 1, which has been distinguished from Janoska at al. for failing to disclose each and every element of claim 1. Accordingly, claims 7 and 9 are paentably distinguishable from Janoska et al. for at least the same reasons as claim 1.

Claims 20 and 22 depend from claim 17, which has been distinguished from Janoska at al. for failing to disclose each and every element of claim 17. Accordingly, claims 20 and 22 are paentably distinguishable from Janoska et al. for at least the same reasons as claim 17

As to claim 18, as explained above, Janoska et al. does not disclose, teach, or suggest a remote memory for storing PDUs. Further, claim 18 depends from claim 17, which has been distinguished from Janoska at al. for failing to disclose each and every element of claim 17. Accordingly, claim 18 is paentably distinguishable from Janoska et al. for at least the same reasons as claim 1.

Claim 21 depends from claim 17, which has been distinguished from Janoska at al. for failing to disclose each and every element of claim 17. Accordingly, claim 21 is paentably distinguishable from Janoska et al. for at least the same reasons as claim 1.

Further as to claim 21, in rejecting the mapping a memory location of a PDU buffered in the remote memory device, the Examiner has stated that in Janoska et al., "the queues are mapped to the partition." This implies that the mapping of a partition is like mapping of a remote memory device. However, in rejecting claim 1, the Examiner stated that "shared portion is seen as the remote" where in figure 5, Janoska et al. shows that the shared portion is part of a partition. Therefore, if the mapping of a partition is like mapping of a remote memory device, then the mapping of a logical queue corresponding to a reserved portion within a partition is also like mapping of a remote memory device because the reserved portions are included in the partition. But as explained above, according to Janoska et al., shared portion and the reserved portion are part of the same partition. Therefore, the mapping of the partition cannot be considered as mapping of a remote memory device. Accordingly, claim 21 is further patentably distinguishable from Janoska et al.

Rejections under USC §103(a)

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janoska et al., US 6,539,024 B1, in view of Miki et al., US 6,453,394 B2. Applicants respectfully traverse these rejections.

Claims 6 and 8 depend from claim 1, which has been distinguished from Janoska et al. for failing to disclose each and every element of claim 1. Therefore, the combination of Janoska et al. ad Miki et al. cannot render claims 6 and 8 obvious.

Further, in the cited sections, Miki et al. describes a dual port memory such as FIFO. The FIFOs are known as First-In-First-Out memory devices. In FIFOs, data is read-out in the order that it was written-in. Janoska et al. describes a priority based array of logical queues in which the data can be written-in or read-out based on the priority of the incoming PDUs. Furthermore, Janoska et al. describes that not only certain portions of a memory device can be allocated as partitions but individual "cells in varying locations are associated through the use of a linked list or other structure to form various partitions within the buffer 100." (*See* col. 5, lines 35-40, emphasis added). Miki et al. does not describe, show, or teach how a dual port memory such as

FIFO can be used to configured partitions including reserved and shared portions using linked list or other similar structure as described by Janoska et al. In fact, the priority-based partition scheme of Janoska et al. teaches away from using the memory structure such as FIFO. Therefore, the combination of Janoska et al. and Miki et al. does not render claims 6 and 8 obvious. Accordingly, claims 6 and 8 are further patentably distinguishable from the cited references.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

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